**THAT WHICH IS CLAIMED IS:**

1. A modulation/demodulation device (10) capable of operating according to a plurality of types of modulation using different carrier frequencies, characterized in that it comprises:

a modulator (12) for modulating (40-46, 58-62), according to the type of modulation, at least one signal at a carrier frequency by a signal of a determined duration and representative of a binary information supplied by a microprocessor (30), said modulated signal being applied to a sending/receiving device (14) for sending to a remote site,

a demodulator (16) for receiving the modulated signals from a remote site via the sending/receiving device (14) and which demodulates said modulated signals by

determining (18, 20, 22, 24) the type of modulation (MA, MB, MC, MD) used for the received signals and their carrier frequency/frequencies (F1, F0),

supplying (220) signals from an analysis of the signals received according to the determined type of modulation, and

detecting the signals of determined duration representative of binary information to make them accessible by the microprocessor.

2. Device according to claim 1,

characterized in that the modulator comprises a generator for generating at least one signal at a carrier frequency (F1, F0), said generator comprising:

a digital type memory (40) which contains R codes representative of a sinusoid,

at least one address counter (CPT1, CPT0) addressing said memory (40), which scans successive addresses of the R codes representative of the sinusoid at the frequency of the pulses from a clock signal, said frequency of the pulses being equal to R times the carrier frequency (F1, F0),

a digital-to-analog converter (58) for converting the R representative codes and supplying an analog signal at the carrier frequency (F1, F0), and

a bandpass filter (60) for eliminating signals at frequencies other than the carrier frequency.

3. Device according to claim 2, characterized in that the generator comprises:

two address counters (CPT1, CPT0) for scanning successive addresses at different frequencies, and

a routing circuit (46) for routing addresses of the two address counters as a function of binary information supplied by the microprocessor (30).

4. Device according to claim 2 or 3, characterized in that the modulator comprises means (50) for counting the number (N, M) of cycles of an

address counter (CPT1, CPT0) and thus determining the duration of the carrier frequency modulation signal (F1, F0).

5. Device according to claim 2, 3 or 4, characterized in that the modulator further comprises means (52, 54) for determining the frequency of pulses of the clock signal applied to the address counter(s) (CPT1, CPT0) as a function of the carrier frequency (F1, F0) and of the number R of samples per sinusoid.

6. Device according to any one of the preceding claims, characterized in that the means allowing the demodulator to determine the type of modulation (MA, MB, MC or MD) of the received signals comprise:

a set of bandpass filters (18) each centered on the carrier frequency/frequencies (F1, F0) of the types of modulation (MA, MB, MC, MD) and which each supply a signal (Vin),

a set of operational amplifiers (20) with gain control for amplifying the signals (Vin) at the output of the bandpass filters (18), and which each supply an output signal (VIN),

a set of comparators (22) for comparing each output signal (VIN) of the amplifiers (20) with a reference signal (Vref) and obtaining a state signal on the output terminal of each comparator (142), and

an encoding circuit (144) for encoding state signals of the comparators to determine the type of

modulation (MA, MB, MC, MD) of the received signals.

7. Device according to claim 6, characterized in that it further comprises a selection circuit (26) for selecting the receiving channel corresponding to the received signal and controlled by the encoding circuit (144).

8. Device according to claim 6 or 7, characterized in that each operational amplifier with gain control (20) comprises:

an operational amplifier (80) with a network of switchable resistors (82) in a feedback circuit for amplifying the signal (Vin),

first, second and third comparators (86, 88, 90) respectively for comparing the signal (Vin) to three thresholds (Vrefnominal, Vrefmini, Vrefmaxi) and supplying state signals according to the result of the comparisons,

a logic unit (92) for combining the state signals of the comparators (86, 88, 90) and delivering or not pulses,

an up/down counter (84) receiving or not the pulses supplied by the logic unit (92) so as to:

increment its content when the signal (VIN) is greater than Vrefmini but less than Vrefnominal and Vrefmaxi,

decrement its content when the signal (VIN) is greater than Vrefmini, Vrefnominal and Vrefmaxi, and

not modify its content when the signal (VIN)

is greater than Vrefmini and Vrefnominal but less than Vrefmaxi,

said up/down counter being connected to the switchable resistor network to modify the feedback resistance.

9. Device according to any one of claims 1 to 8, characterized in that the means for supplying the analysis signals of the received signal comprise a clock circuit (220) which generates at least one pulse signal whose frequency is R times the carrier frequency of the signal being received.

10. Device according to claim 9, characterized in that the means for detecting the signals of a determined duration and representative of binary information comprise:

means (200, 202, 204) for sampling and encoding the amplitude of the samples of the received signal (Vin) into representative codes,

means (206, 210 and 230) for counting the samples and determining the period of the received signal,

means (240) for counting the number of periods of the received signal and determining whether this corresponds to a digit "1" or "0", and

means (254) for recording the succession of "1" and "0" digits.

11. Device according to claim 10,

characterized in that the means for sampling and encoding the amplitude of samples comprise:

a circuit (200) for translating and shaping the received signal,

a circuit (202) for sampling the translated and shaped signal, and

an analog-to-digital converter (204) for converting codes representative of the amplitude of the samples.

12. Device according to claim 10 or 11, characterized in that the sample counting means (230) comprise:

a comparator (206) for comparing the codes of the samples with a code representative of a threshold (Vref) and supplying a state signal when the amplitude of the sample is greater than the threshold (Vref),

a latch (208) for storing the state signal supplied by the comparator (206),

a sample counting circuit (212, 218), and

a comparator (222) for comparing the counted number of samples to the expected number and supplying a validation signal when the numbers are equal.

13. Device according to claim 10, 11 or 12, characterized in that the means (240) for counting the number of periods of the received signal and determining whether it corresponds to a "1" digit or a "0" digit comprise:

a counter (242) for the number of periods of

the received signal,

a first comparator (244) for comparing the counted number to the number N of periods for a "1" digit and supplying a validation signal for the binary digit "1" if the two numbers are equal, and

a second comparator (248) for comparing the counted number to the number M of periods for a digit "0" and supplying a validation signal for the digit "0" if the two numbers are equal.

14. Device according to any one of claims 6 to 13, characterized in that said set of bandpass filters is formed by switched capacitor type filter means to obtain the different operating frequencies.

15. Device according to any one of claims 6 to 14, characterized in that said set of operational amplifiers is formed by switched capacitor amplifier means to obtain the different operating frequencies.

16. Device according to claim 15, characterized in that said switched capacitor operational amplifier means is connected to the output terminal of the selection circuit (26).